(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 300 869 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
09.04.2003 Bulletin 2003/15

(51) Int Cl.[7]: **H01J 17/04**, H01J 17/49, H01J 9/02, C23C 14/08

(21) Application number: **02026763.9**

(22) Date of filing: **05.11.1997**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **30.05.1997 JP 14134897**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
97308899.0 / 0 881 657

(71) Applicant: **FUJITSU LIMITED**
Kawasaki-shi, Kanagawa 211-8588 (JP)

(72) Inventors:
- **Nakahara, Hiroyuki**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Katayama, Takashi**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Ishimoto, Manabu**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Iwase, Nobuhiro**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Hidaka, Souichirou**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Mochizuki, Akihiro**
  Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- **Iwasaki, Kazuhide,**
  Kyushu Fujitsu Electronics Ltd.
  Satsuma-gun, Kagoshima 895-14 (JP)

(74) Representative: **Hitching, Peter Matthew et al**
Haseltine Lake & Co.,
Imperial House,
15-19 Kingsway
London WC2B 6UD (GB)

Remarks:
This application was filed on 02 - 12 - 2002 as a divisional application to the application mentioned under INID code 62.

(54) Plasma display panel

(57) A substrate assembly for a plasma display panel, comprises a substrate (11), a plurality of surface-discharge electrodes (X,Y) extending over the substrate (11), and a dielectric layer (17) covering the surface-discharge electrodes (X,Y). A magnesium oxide film (18) extends over the dielectric layer (17) to provide the substrate assembly with a surface that is to be in contact with a discharge gas. The magnesium oxide film (18) contains silicon or a compound thereof, at an amount of 500 to 10,000ppm by weight, to reduce an occurrence of black noise in operation of the plasma display panel.

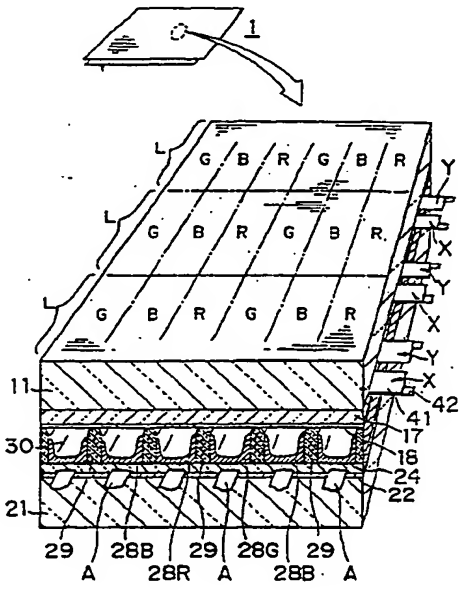


Fig. 4

EP 1 300 869 A1

Description

[0001] The present invention relates to plasma display panels (PDPs), especially AC-type plasma display panels operable in matrix display systems. One embodiment of the present invention can provide a plasma display panel suitable for use as a surface discharge type PDP in which discharge will occur along a screen.

[0002] Recently, plasma display panels (PDPs) have been widely used in television displays as well as monitors of computers now that colour PDP screens are commercially available. Particularly, these PDPs may be utilized as large-screen flat type display devices for the high definition television (HDTV) system.

[0003] In matrix display type PDPs, a memory effect is utilized so as to sustain lighting conditions of cells. The AC type PDP has a memory function by virtue of its structure in which an electrode is covered with a dielectric material. That is, when the AC type PDP is turned ON, lines are successively addressed in order to store wall electron charges only into cells to be lit (emit light). Thereafter, voltages (namely sustain voltages) having alternate polarities are applied to all of these cells within a time period. This sustain voltage corresponds to a predetermined voltage lower than a discharge starting voltage. In such a cell where wall electron charges are stored, since the wall voltage is superimposed with the sustain voltage, the effective voltage applied to this cell exceeds the discharge starting voltage, so that a discharge operation will occur. If the time period during which the sustain voltage is applied is shortened, then a virtually continuous lighting condition can be obtained.

[0004] In surface discharge type PDPs which are commercially available, pairs of sustain electrodes (namely, first electrodes and second electrodes) are arranged in parallel to each other. The pairs of first and second electrodes extend over an entire length of the screen in a matrix display with one pair for every line (row), whereas address electrodes (namely, third electrodes) are arranged with one electrode for every column. An interval between sustain electrodes in the respective lines is referred to as a "discharge slit". A width of this discharge slit is selected to be such a value, for example 50 to 100 μm, that the surface discharge may occur when an effective voltage of on the order of 200 to 250 V is applied. On the other hand, another interval between sustain electrodes present in adjacent lines is referred to as a "reverse slit". A width of this reverse slit is made sufficiently larger than that of the discharge slit. That is to say, the reverse-slit width is made large enough that occurrence of surface discharge between the sustain electrodes separated from each other via the reverse slit can be prevented. As described above, both the discharge slit and the reverse slit are provided in the arrangement of the sustain electrodes, so that the respective lines can be selectively emitted (activated).

[0005] A protection film having an anti-sputtering characteristic capable of mitigating an influence caused by ion bombardment occurring during discharge operation is provided on a surface of a dielectric material layer (for instance, a low melting point glass) for covering the sustain electrodes. Since this protection film is in contact with the discharge gas, both a material of this protection film and a film quality thereof may have a great influence on the discharge characteristic. In general, magnesium oxide is employed as a protection film material. Magnesium oxide is an insulating material having a superior anti-sputtering characteristic and a large secondary electron emission coefficient. In other words, when magnesium oxide is used, the discharge starting voltage is lowered, so that the surface discharge type PDP can be readily driven. Recently, a magnesium oxide film having a thickness of on the order of 1 μm is formed on a surface of the dielectric material layer by performing a vacuum vapor deposition while using magnesium oxide made in a pellettform as a starting material.

[0006] US 5454861 discloses a substrate assembly for a plasma display panel which may be considered to comprise: a substrate; a plurality of surface-discharge electrodes extending over the substrate; a dielectric layer covering the surface-discharge electrodes; and a magnesium oxide film extending over the dielectric layer to provide the substrate assembly with a surface that is to be in contact with a discharge gas when the substrate assembly is in use. A composition for forming the magnesium oxide film comprises magnesium oxide particles and, as a binder precursor, one or more organic compounds containing aluminium, silicon, titanium or zirconium. This composition can be coated on the dielectric layer and then fired to convert the binder precursor to the metal oxide, thereby avoiding the need to use a vacuum deposition method to form the film.

[0007] When the surface discharge type PDP is driven, a charge distribution over an entire screen is initialised (reset) during a time period commencing after the sustain voltage application for a certain image is accomplished and ending before a next image is addressed. Concretely speaking, prior to the addressing operation, reset pulses whose peak values exceed the discharge starting voltage are applied to the sustain electrode pairs of all of the lines. When the reset pulses are applied, the surface discharge phenomenon will occur at leading edges of these reset pulses, so that a large amount of wall electron charges are charged to the respective cells compared to the charging brought about by the sustain voltage application. Subsequently, the self-discharge phenomenon will occur, which is caused only by the wall voltage, in response to the trailing edges of the reset pulses. As a result, the most wall charges are neutralized, and thus will disappear. In other words, the dielectric materials over the entire screen are brought into a substantially non-charged condition. Alternatively, another initialization may be carried out without such a self-discharge operation by causing an erasing/discharge phenomenon to occur only in the cells which have been previously, selectively

charged. In this alternative case, an addressing operation is required for this initialization, so that a time required for switching images may be prolonged.

[0008] Conventionally, there is another problem which results in a displayed image being disturbed. This problem may be referred to as "black noise". The "black noise" is a phenomenon in which a cell to be lit (namely, selected cell) cannot be lit. This black noise may easily occur in a boundary between a lit region and a non-lit region within a screen. It is not the case that all of the plural selected cells contained in either one line or one column are not lit. However, since the black noise occurrence portions appear in some places, it may be understood that black noise occurs as a consequence of an address missing phenomenon. This address missing phenomenon is caused when no address discharge operation is executed, or even when an address discharge operation is performed but the strength thereof is low.

[0009] One possible reason why the address missing phenomenon occurs is considered to be the residual wall charges in the reverse slit. In the case that the surface discharge operation is excessively spread by the applied reset pulses and thus the wall charges are stored also in the reverse slit, even when the self-erasing discharge operation is subsequently performed, the wall charges present at the reverse slit located far from the discharge slit are left. The effective voltage of the addressing operation is lowered by this residual charge, so that the address missing phenomenon will occur in some cells selecting during the addressing operation. If the neighboring cells are also selected cells, since the space charges caused by the address discharge operations at the neighboring cells may contribute the priming effect, the address missing phenomenon is unlikely to occur. On the contrary, in the case that the neighboring cells (especially, cells ahead in the scanning sequence) are non-selected cells as in the above-described boundary, no priming effect may occur. Thus, in this case the address missing phenomenon may sometimes occur.

[0010] It is therefore desirable to solve the above-described problems, and to reduce an occurrence ratio of a so-called "black noise".

[0011] One embodiment of the present invention can provide a plasma display panel of a matrix display type, having a first electrode and a second electrode which constitute a main electrode pair, the first electrode and the second electrode being covered with an insulating layer against a discharge gas, wherein the insulating layer comprises a magnesium oxide film formed at least as a surface layer thereof which is in contact with the discharge gas, the magnesium oxide film having an impedance in the range of 230 to 330 $k\Omega/cm^2$ at a frequency of 100Hz.

[0012] Another embodiment of the present invention can provide a plasma display panel of a matrix display type, having a first electrode and a second electrode which constitute a main electrode pair, the first electrode and the second electrode being covered with an insulating layer against a discharge gas, wherein the insulating layer comprises a magnesium oxide film formed at least as a surface layer thereof which is in contact with the discharge gas, the magnesium oxide film containing silicon atom or a compound thereof at an amount of 500 to 10,000 weight ppm.

[0013] A plasma display embodying a second aspect of the present invention comprises: a plasma display panel of a matrix type, having a first electrode and a second electrode which constitute a main electrode pair and are formed on a same plane, a third electrode being formed so as to intersect with the first electrode and the second electrode, the first electrode and the second electrode being covered with an insulating layer against a discharge gas, wherein the insulating layer comprises a magnesium oxide film formed at least as a surface layer thereof which is in contact with the discharge gas, the magnesium oxide film having an impedance in the range of 230 to 330 $K\Omega/cm^2$ at a frequency of 100 Hz, or containing silicon atom or a compound thereof at an amount of 500 to 10,000 weight ppm and

a drive apparatus for applying a reset voltage between the first electrode and the second electrode during an initializing time period, applying an address voltage between the second electrode and the third electrode during an address time period, and applying a sustain voltage between the first electrode and the second electrode during a sustain time period, whereby both an addressing operation and a sustain operation are performed after a charging distribution of the entire screen has been initialized by self-erasing discharge.

[0014] A substrate assembly for a plasma display panel, embodying a third aspect of the present invention, comprises;

a substrate;

a plurality surface-discharge electrodes on the substrate;

a dielectric layer covering the surface-discharge electrodes; and

an insulating layer covering the dielectric layer,

wherein the insulating layer comprises a magnesium oxide film formed as a surface layer thereof on a side which is to be in contact with a discharge gas, the magnesium oxide film having an impedance in the range of 230 to 330 $k\Omega/cm^2$ at a frequency of 100 Hz, or containing silicon atom or a compound thereof at an amount of 500 to 10,000 weight ppm.

[0015] In one embodiment, the magnesium oxide film is formed in such a manner that:

magnesium oxide in a pellet form is mixed with a starting material of an impurity in a pellet or powder form, and the mixture is heated at the same time;

a sintered member of a mixture of magnesium oxide in a powder form and a starting material of an impurity in a powder form is heated so as to be vapor-deposited; or
a sintered member of a mixture of magnesium oxide in a powder form and a starting material of an impurity in a powder form is used as a target for sputtering,
whereby the magnesium oxide film having an impedance in the range of 230 to 330 kΩ/cm^2 at a frequency of 100 Hz is formed, or the magnesium oxide film containing silicon atom or a compound thereof at amount of 500 to 10,000 weight ppm is formed.

[0016] Reference will now be made, by way of example, to the accompanying drawings, in which:

Fig. 1 is a schematic block diagram for representing a structure of a plasma display device (PDP) embodying the present invention;
Fig. 2 schematically illustrates a frame division used in the PDP of Fig. 1;
Fig. 3 illustratively represents a voltage waveform diagram for describing a drive sequence of the PDP shown in Fig. 1;
Fig. 4 is a perspective view for representing an internal structure of a PDP embodying the present invention;
Fig. 5A and Fig. 5B illustrate a method for measuring an impedance;
Fig. 6 is a graphic representation illustrating a relationship between impedance of a magnesium oxide film and image quality; and
Fig. 7 is a graphic representation illustrating a relationship between a contained amount of silicon and the image quality.

[0017] As previously described, one embodiment of the present invention is intended to reduce the occurrence ratio of a so-called "black noise", namely cells to be lit cannot be lit, and further to improve display qualities of a PDP (plasma display panel). To this end, one PDP embodying the present invention has a structure in which a surface to be in contact with discharge gas, typically a surface of a dielectric layer for electrodes is covered by a magnesium oxide film having a specific film quality. By employing this structure, a discharge characteristic of the PDP can be improved.

[0018] The film quality of the magnesium oxide film will depend upon a film forming condition containing a composition of a starting material. The following recognitions have been made. An occurrence ratio (degree) of the so-called "black noise" was found from comparison results to have a definite dependence upon manufacturing lot . To specify electrical characteristics, impedances were measured. The reason why the impedances are measured is such that it is very difficult to correctly measure a DC resistance value of an insulating material.

[0019] The following results have been obtained. That is, when the impedance value is within a predetermined range, the occurrence degree of the black noise is low, whereas when the impedance value is outside (smaller or larger than) the predetermined range, the occurrence degree of the black noise is high.

[0020] Also, a composition analysis of the magnesium oxide has been carried out. In the case that the contained amount of silicon (Si) atom is within a predetermined range, the occurrence degree of the black noise is low. In the case of boron (B) atom, carbon (C) atom and calcium (Ca) atom, there is no particular difference between a sample having a high occurrence ratio of the black noise, and a sample having a low occurrence ratio of the black noise. It could be predicted that an element whose valence is larger than (more than) or equal to 3 (the valence of magnesium which is the same as silicon) would provide similar effects to the silicon atom, in particular, elements in the 3a group or 4a group, the ion radius of which is close to that of magnesium.

[0021] In this specification, a "predetermined range" means a range defined from 230 kΩ/cm to 330 kΩ/cm.

[0022] It is preferable that the magnesium oxide film contains either an element whose valence is larger than or equal to 3, or a compound thereof, as an impurity. The impurity may be selected from silicon atom, aluminum atom, or a compound of these elements. Either silicon atom or its compound such as silicon oxide is preferably contained in the magnesium oxide film within a range of 500 to 10,000 weight ppm.

[0023] Further, one possible reason why the address missing phenomenon which causes black noise can be suppressed is as follows: projection amounts of secondary electrons are increased, so that lowering of an effective voltage caused by residual charges can be compensated. The residual effect of electron charges can be reduced, and the residual charges can quickly disappear.

[0024] Next, a description will now be made of a method for manufacturing the magnesium oxide film.

[0025] As the starting material of the magnesium oxide film, magnesium oxide formed in either a pellet or powder may be employed. In the case in which an impurity is contained in this magnesium oxide film, a starting material of this impurity may be formed in either a pellet or powder.

[0026] The magnesium oxide film may be manufactured by employing the above-described starting material in either a vapor depositing method or a sputtering method, as exemplified as follows.

(1) In one vapor deposition method, magnesium oxide formed in a pellet is mixed with the starting material of the impurity formed in a pellet or powder, and these starting materials are heated at the same time so as to be vapor-deposited.

(2) In another vapor deposition method, a sintered member is made of a mixture between magnesium oxide formed in powder and the starting material of the impurity formed in powder is heated so as to be vapor-deposited.

(3) In a sputtering method, a sintered member is made of a mixture between magnesium oxide formed in power and the starting material of the impurity formed in powder, and this sintered member is used as a target for sputtering. It should be noted that in accordance with another aspect of the present invention, not only the PDP, but also a substrate assembly used for the PDP can provided. Such a substrate assembly used for the PDP embodying the present invention is, in the case of a surface discharged type PDP for example, a substrate assembly provided on the display side.

[0027] Also, a structure of an electrode employed in a PDP embodying the present invention may have a first electrode and a second electrode, which constitute a main electrode pair (a surface-discharge electrodes) formed on the same plane, usually a same substrate, and further a third electrode which intersects with the first electrode and the second electrode. It should also be noted that the third electrode may be used as a so-called "address electrode" to which an address voltage is applied.

[0028] Further, in an embodiment of the present invention, a plasma display device may be provided which is constructed of the above-described PDP and a drive apparatus thereof.

[0029] Although the present invention is not limited to the below-mentioned drive apparatus, such a drive apparatus may be provided in which a reset voltage is applied between the first electrode and the second electrode during an initializing time period, an address voltage is applied between the second electrode and the third electrode during an address time period, and a sustain voltage is applied between the first electrode and the second electrode during a sustain time period. As a consequence, after the charging distribution of the entire screen has been initialized by self-erasing discharge, both an addressing operation and a sustain operation can be performed.

[0030] Fig. 1 is a schematic block diagram showing a plasma display device 100 embodying the present invention.

[0031] The plasma display device 100 is arranged by an AC type PDP 1 functioning as a matrix type color display device and a drive unit 80 for selectively lighting a large number of cells which constitute a display screen. This plasma display device 100 may be used as a wall-mounted type television, and a monitor of a computer system.

[0032] The AC type PDP 1 is a surface discharge type PDP in which one pair of sustain electrodes X and Y (the first electrode and the second electrode) are arranged in parallel to each other. Each of cells in this PDP 1 has an electrode matrix having a three-electrode structure corresponding to the sustain electrodes X, Y and the address electrode (third electrode). The sustain electrodes X and Y extend along a line direction (horizontal direction) of the screen, and one sustain electrode (the Y electrode) is employed as a scan electrode for selecting the cells of a line as one unit when an addressing operation is performed. The address electrode "A" is a data electrode for selecting the cells of a column as one unit, and extends along a column direction (vertical direction).

[0033] The drive unit 80 contains a controller 81, a frame memory 82, an X-driver circuit 86, a Y-driver circuit 87, an address driver circuit 88, and a power supply circuit (not shown in detail). Picture (video) data DR, DG, DB having multiple values, which indicate luminance levels (gradation levels) of R, G, B signals for each pixel are supplied to this drive unit 80 from an external apparatus in combination with various sorts of synchronization (sync) signals. The picture data DR, DG, DB are first stored in the frame memory 82, and then are converted into sub-frame data "Dsf" every color by the controller 81. These sub-frame data Dsf are also stored in the frame memory 82. This sub-frame data Dsf corresponds to a set of binary data for indicating (in order to display gradation - see below) whether or not the cells are required to be lit in respective sub-frames produced by subdividing one frame. The X-driver circuit 86 functions to apply a voltage to the sustain electrode X, and the Y-driver circuit 87 functions to apply a voltage to the sustain electrode Y. The address driver circuit 88 selectively applies an address voltage to the address electrode A in response to the sub-frame data Dsf transferred from the frame memory 82.

[0034] Next, a description will now be made of a driving method applicable to this PDP 1.

[0035] Fig. 2 schematically represents a frame division, and Fig. 3 is a voltage waveform diagram for indicating a drive sequence.

[0036] To reproduce gradation by binary-controlling emissions of cells, each frame "F" in a time sequence of frames corresponding to an externally inputted image is subdivided into, for instance, 6 sub-frames sf1, sf2, sf3, sf4, sf5, and sf6. A relative ratio of illuminance in the respective sub-frames sf1 to sf6 is set to be equal to 1:2:4:8:16:32, and the number of sustain pulses applied to the sustain electrodes in each of the sub-frames sf1 to sf6 is set accordingly. Since 64 luminance step levels "0" to "63" can be set with respect to each of the R, G, B colors by combining ON/OFF operations of emissions in unit of the sub-frame, a total number of displayable colors becomes 643. It should be understood that there is no need to display these sub-frames sf1 to sf6 in a sequence of the relative ratio of luminance. For example, the subframe sf6 having the large relative ratio may be arranged at an intermediate portion of the display

period so as to realize optimization.

[0037] As indicated in Fig. 3, with respect to each of the sub-frames sf1 to sf6, a reset time period "TR", an address time period "TA", and a sustain time period "TS" are allocated. The lengths of the reset time period TR and the address time period TA are made constant irrespective of the relative ratio of luminance, whereas the larger the relative ratio of luminance becomes, the larger the length of the sustain time period TS becomes. In other words, the lengths of the display time periods of the respective sub-frames sf1 to sf6 are different from each other.

[0038] The reset time period TR corresponds to a time period during which wall charges of an entire screen are erased (initialized) in order to prevent an adverse influence caused by cells which were in a lit state in the preceding operation. A reset pulse "Pw" having a positive polarity, the peak value of which exceeds the surface discharge starting voltage, is applied to the sustain electrodes X of all of the lines (line numbers being "n"), and at the same time, a pulse having a positive polarity is applied to all of the address electrodes A in order to avoid charging on the rear surface and ion bombardment. In response to a rising portion of the reset pulse Pw, a strong surface discharge will occur in all of the lines, so that a large amount of wall electron charges are produced in each cell. The applied voltage is canceled by this wall voltage, so that the effective voltage is lowered. When the reset pulse Pw rises, the wall voltage directly becomes the effective voltage, so that the self-discharge phenomenon will occur. The majority of the wall charge at all of the walls may disappear, and thus the overall screen is brought into a uniform non-charged condition.

[0039] The address time period TA corresponds to a time period of an addressing operation (namely, setting of lit/non-lit). The sustain electrode X is biased to have a positive potential with respect to the ground potential, and all of the sustain electrodes. Y are biased to have a negative potential. Under this condition, the respective lines are sequentially selected one line at a time from a top line to a last line, and then a scan pulse "Py" having a negative polarity is applied to the relevant sustain electrode Y. When the lines are selected, at the same time, an address pulse "Pa" having a positive polarity is applied to the address electrode A corresponding to a cell which is indicated by the sub-frame data Dsf as a cell that should be lit. In the selected line, a counter discharge will occur between the sustain electrode Y and the address electrode A at the cell, to which the address pulse Pa is applied, and then this counter discharge is advanced to a surface discharge. A series of the above-described discharge operations corresponds to an address discharge operation. Since the sustain electrode X is biased to a potential of the same polarity as the address pulse Pa, the effect vis-a-vis the sustain electrode X of the pulse Pa is canceled by this biassing potential, so that no discharge operation can be produced between the sustain electrode X and the address electrode A.

[0040] The sustain time period TS corresponds to a time period during which a preset lighting state is maintained so as to secure luminance in response to a gradation level. To prevent an unnecessary discharge operation, all of the address electrodes A are biased to a potential of a positive polarity, and a sustain pulse Ps having a positive polarity is applied to all of the sustain electrodes Y at the beginning of the period TS. Thereafter, sustain pulses Ps are alternately applied to the sustain electrode X and the sustain electrode Y, the surface discharge will occur at the cells where the wall charges are stored during the address time period TA every time the sustain pulse Ps is applied. The application time period of the sustain pulse Ps is constant, and the number of sustain pulses Ps which are applied is set based upon the relative ratio of the luminance.

[0041] Fig. 4 is a perspective view for illustrating an internal structure of a PDP 1 embodying the present invention.

[0042] In this PDP 1, a pair of sustain electrodes X and Y is arranged for every line L (corresponding to a row of cells) of a screen, each electrode extending along a horizontal direction on an inner surface of a glass board 11. The board 11 and a further board 21 constitute a pair of boards for sandwiching a discharge space 30, the board 11 being provided on a front surface side. Each of the sustain electrodes X and Y is made of a metal film 42, in order to reduce a resistance value, in combination with a transparent conductive film 41, and is covered with a dielectric layer 17 for an AC drive purpose. A material of the dielectric layer 17 is a PbO group low melting point glass (dielectric constant is approximately 10). A magnesium oxide film 18 (a film quality of the film 18 will be discussed later) is coated as a protection film on a surface of the dielectric layer 17. A thickness of this magnesium oxide film 18 is 5000~9000Å, e. g. approximately 7,000 Å. Both the dielectric layer 17 and the magnesium oxide film 18 have light transmission characteristics. It should be noted that a board on which a stacked layer member constructed of sustain electrodes, the dielectric layer, and the protection film may be referred to as a board for a plasma display panel. An under base layer 22, address electrodes A, an insulating layer 24, isolation walls 29, and three colors (R, G, B) fluorescent material layers 28R, 28G, 28B for color display are formed on an inner surface of the glass board 21 provided on the rear surface side. Each of the isolation walls 29 has a straight line form, while observing on a flat surface. The discharge space 30 is sub-divided in the line direction by these isolation walls 29 into sequently corresponding to every sub-pixel (namely, unit light emitting region),

and further an interval between the adjoining segments of discharge space 30 is defined as a predetermined value (about 150 μm). A discharge gas made by mixing a very small amount of xenon with neon is filled into the discharge space 30. The fluorescent material layers 28R, 28G, 28B are locally excited by ultraviolet rays produced during discharge operation to emit visible light having preselected colors.

[0043] A single display pixel is provided by three sub-pixels arrayed along the line direction. A structural member

within a range of the respective sub-pixels corresponds to the cell. Since the barrier ribs 29 are arranged in a stripe pattern, the discharge space 30 has portions, corresponding to the respective columns, which are continuous along the column direction, i.e. these portions bridge all lines. The colors emitted from the sub-pixels within the respective columns are equal to each other.

[0044] The PDP 1 of the above-described structure is manufactured by carrying out a series of the below-mentioned manufacturing steps. That is, a predetermined structural element is separately provided on each of the glass boards 11 and 21 to thereby form substrate assemblies for a front surface and a rear surface. Both the substrate assemblys are overlapped with each other with a predetermined space therebetween, peripheral portions of the space are sealed, air in the space is exhausted, and the discharge gas is filled into the space. While the substrate assembly for the front surface is manufactured, the magnesium oxide film 18 is formed under a condition selected such that the film quality capable of effectively reducing the black noise can be obtained.

[0045] Now, a description will be made of the film quality of the magnesium oxide film 18.

[0046] Fig. 5A and Fig. 5B illustratively show a method for measuring an impedance. Fig. 6 is a graphic representation of a relationship between an impedance of a magnesium oxide film and an image quality.

[0047] First, a plurality of electrode boards are prepared. Magnesium oxide films were formed on the surfaces of these electrode boards under different film forming conditions. As indicated in Fig. 5A, an electrode board 91 is manufactured in such a manner that a conductive film 93 constituted by an electrode portion 93a having a diameter of 20 mm and a conducting portion 93b is formed on a surface of glass plate 92 with a size of 50 mm×60 mm. A material of the conductive film 93 is selected to be ITO which is the same as the transparent conductive film 41 for constituting the sustain electrodes X and Y. After a magnesium oxide film 95 having a thickness of approximately 7,000 Å was formed in such a manner that the entire portion of the electrode portion 93a could be uniformly covered, as represented in Fig. 5B, another electrode board 91 was overlapped, and then the magnesium oxide film 95 was sandwiched by employing one pair of conductive films 93. Subsequently, an impedance of the resultant magnesium oxide film 95 was measured by using an LCR meter. The measuring conditions were given as follows: the weight for sandwiching the magnesium oxide film 95 was 7 kg/cm^2; the applied voltage was 1 V (effective value), and the frequency was 100 Hz.

[0048] On the other hand, impedances of a plurality of samples were measured, and at the same time, an image quality of the PDP on which the magnesium oxide film 18 has been formed was evaluated. This evaluation was carried out by way of an observation investigation while displaying a transverse stripe pattern in which lighting line groups and non-lighting line groups were alternately arranged every several tens of lines. A luminance level of the lighting line group was made equal to a half of a maximum luminance level, namely about "32". The black noise was made noticeable by lighting only the sub-frames sf6 whose relative rate was "32". If the number of sub-frame to be lit is equal to 1, then one address missing phenomenon may appear as the entire frame is lit. Also, when the luminance level is equal to "32", there is a large luminance difference in such a case that a frame is correctly lit, and is not correctly lit. When the respective lines are sequentially selected from the topline to the last line to perform the addressing operation in the above-described manner, the black noise may readily occur at a line located at the nearest position with respect to the top line of each of the lighting line groups. It should be noted that since the address missing phenomenon does not always occur, the black noise can be recognized as a flicker phenomenon in the light emission.

[0049] As to image qualities of the respective PDPs manufactured as a sample, the evaluation was carried out with six evaluation levels as shown in Table 1 below so as to investigate a relationship between impedances and image qualities.

Table 1

Evaluation Level/Flickering Degree
5 (best) ---no flicker
4---flicker intermittently occurs in several cells
3---flicker substantially normally occurs in several cells
2---flicker normally occurs in most of cells in 1 line
1---flicker normally occurs in most of cells in 2 lines
0 (worst)--flicker normally occurs in most of cells in more than 3 lines

[0050] As apparent from the graphic representation shown in Fig. 6, the best image quality can be obtained in a range that the impedance per 1 cm^2 is 270 to 300 kΩ. Conversely, the image qualities are deteriorated when the impedance is lowered from this range, and also increased from this range. When the image quality becomes lower than the evaluation level 2, the characters can be hardly read. However, when the image quality becomes higher than the evaluation level 3, there is no practical problem. In other words, the allowable range of the impedance corresponding to a good image quality range is 230 to 330 kΩ.

[0051] Fig. 7 is a graphic representation for showing a relationship between an image quality and a contained amount

of silicon.

[0052] A sample was manufactured by forming a magnesium oxide film on a tantalum board. The investigation was made of compositions of the magnesium oxide film with respect to a region of a plane area of 450 cm^2 by way of the emission analysis method (ICP method). When the magnesium oxide film was formed on the tantalum board, at the same time, the magnesium oxide film 18 was formed, so that the PDP was manufactured in the same way as the sample. The image qualities of the sample PDPs were evaluated in a similar evaluation manner to the above-described evaluation manner. As represented in Fig. 7, an allowable range of silicon atom concentration corresponding to a good image quality range is 500 to 10,000 weight ppm, and the best image quality can be obtained in a range of 1,000 to 8,000 weight ppm. It should be noted that a substantially similar result to the sample analysis by the ICP method could be obtained when the compositions of the magnesium oxide films formed on each of the sample PDPs were investigated by secondary ion mass spectrometry (SIMS).

[0053] The magnesium oxide film 18 containing a proper amount of silicon atom could be obtained by using the vacuum vapor deposition. When the film is formed, magnesium oxide in a pellet and a silicon compound (silicon oxide, silicon monoxide) in a pellet or powder are mixed and the mixture is used as a vapor deposition source. For instance, the magnesium oxide film 18 having the silicon atom concentration of 1,400 weight ppm corresponding to the best evaluation level 5 could be obtained in accordance with the following conditions. That is, a material was used which was made by mixing the silicon oxide powder in the ratio of 0.1 weight % with the magnesium oxide pellet whose grain diameter was 5 to 3 mm and whose purity was higher than, or equal to 99.95%. The magnesium oxide film 18 was manufactured under the following film - forming conditions: the vacuum degree was 5×10^{-5} Torr; the oxygen conduction flow rate was 12 sccm; the oxygen partial pressure was higher than, or equal to 90%; the rate was 20 Å/sec; the film thickness was 7,000 Å; and the board temperature was 150°C by way of the reactive EB vapor deposition method where the pierce type gun was employed as the heat source. Alternatively, a sintered member of a mixture made from magnesium oxide and the silicon compound may be employed as the vapor deposition source. Also, while a similar sintered member may be used as a target in the sputtering operation, a desirable magnesium oxide film 18 may be formed.

[0054] In embodiments of the present invention, the occurrence ratio of the black noise (namely, a phenomenon that a cell to be lit could not be, lit) can reduced, so that the display quality can be improved.

Claims

1. A substrate assembly for a plasma display panel, comprising:

   a substrate (11) ;
   a plurality of surface-discharge electrodes (41, 42) extending over the substrate;
   a dielectric layer (17) covering the surface-discharge electrodes; and
   a magnesium oxide film (18) extending over the dielectric layer to provide the substrate assembly with a surface that is to be in contact with a discharge gas, the magnesium oxide film containing silicon or a compound thereof at an amount of 500 to 10,000 ppm by weight, thereby to reduce an occurrence of black noise in operation of the plasma display panel.

2. A substrate assembly as claimed in claim 1, having an insulating layer covering the dielectric layer, which insulating layer comprises a magnesium oxide film formed as a surface layer thereof on a side which is to be in contact with said discharge gas.

3. A substrate assembly as claimed in claim 1,
   wherein said magnesium oxide film (18) is formed on a surface of said dielectric layer (17).

4. A substrate assembly as claimed in claim 1, 2 or 3, wherein the silicon compound is silicon oxide.

5. A substrate assembly as claimed in any preceding claim, wherein the magnesium oxide film has a thickness of 5000-9000Å.

6. A plasma display panel of a matrix display type, comprising a substrate assembly as claimed in any preceding claim, said plurality of electrodes including a first electrode (X) and a second electrode (Y) which constitute a main electrode pair.

7. A plasma display panel as claimed in claim 6, having a third electrode (A) formed so as to extend across the first

electrode (X) and the second electrode (Y).

8. A plasma display device comprising:

a plasma display panel as claimed in claim 7; and
a drive apparatus (80) for applying a reset voltage (Pw) between the first electrode (X) and the second electrode (Y) during an initialising time period (TR), applying an address voltage (Pa) between the second electrode and the third electrode during an address time period (Ta), and applying a sustain voltage (Ps) between the first electrode (X) and the second electrode (Y) during a sustain time period (TS), whereby both an addressing operation and a sustain operation are performed after a charging distribution of the entire screen has been initialised by self-erasing discharge.

9. A method of manufacturing the plasma display panel of claim 6 wherein magnesium oxide in a pellet form is mixed with a starting material of silicon or a compound thereof in a pellet or powder form, and the mixture is heated at the same time.

10. A method of manufacturing the plasma display panel of claim 6 wherein a sintered member of a mixture of magnesium oxide in a powder form and a starting material of silicon or a compound thereof in a powder form is heated so as to be vapor-deposited.

11. A method of manufacturing the plasma display panel of claim 6 wherein a sintered member of a mixture of magnesium oxide in a powder form and a starting material of silicon or a compound thereof in a powder form is used as a target for sputtering.

12. A method of reducing occurrence of black noise in a plasma display panel in which a plurality of surface-discharge electrodes (41, 42) extend over a substrate (11), a dielectric layer (17) covers the surface-discharge electrodes and a magnesium oxide film (18) extends over the dieletric layer as a surface layer in contact with a discharge gas, which method comprises setting an amount of silicon or a compound thereof contained in the magnesium oxide film in the range from 500 to 10,000 ppm by weight.

13. Use of a magnesium oxide film containing silicon or a compound thereof at an amount in the range from 500 to 10,000 ppm by weight as a surface layer in contact with a discharge gas in a plasma display panel to reduce occurrence of black noise, the panel having a plurality of surface-discharge electrodes (41,42) extending over a substrate (11) and a dielectric layer (17) covering the surface-discharge electrodes, said magnesium oxide film (18) extending over the dielectric layer.

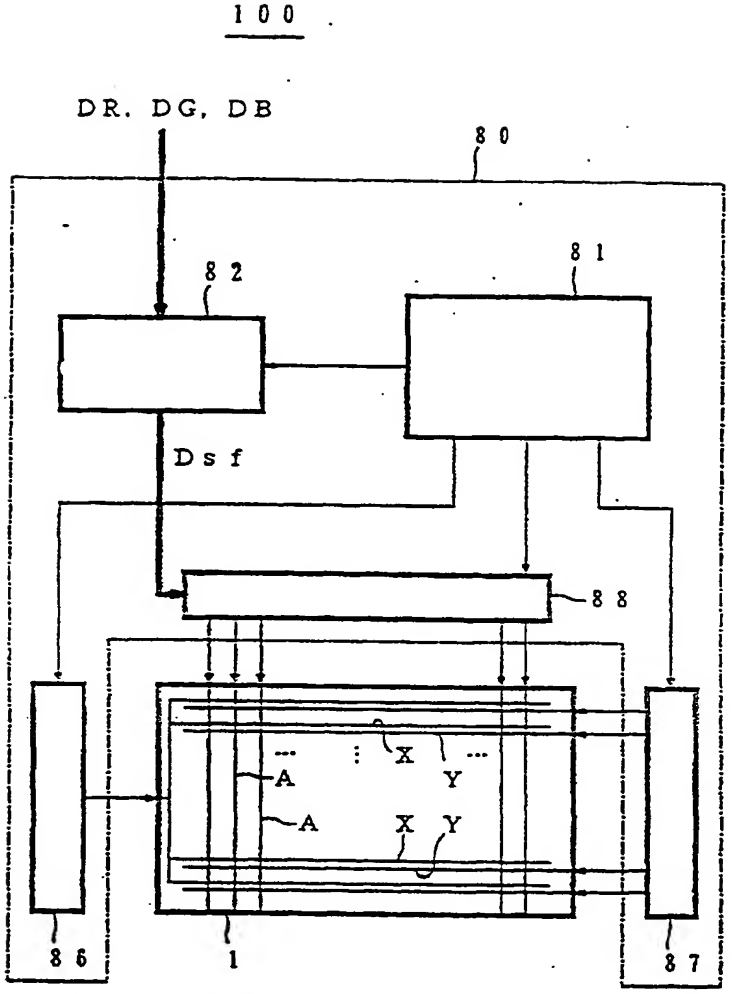


Fig. 1

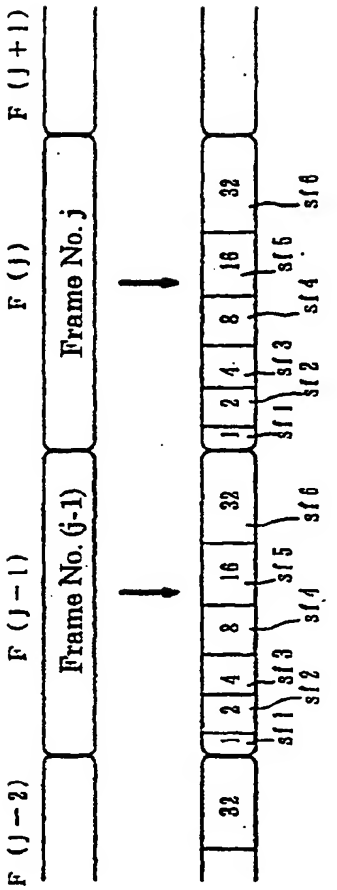

F (J-2)
F (J-1)
F (J)
F (J+1)
Frame No. (j-1)
Frame No. j
32
1
2
4
8
16
32
s11
s12
s13
s14
s15
s16

Fig. 2.

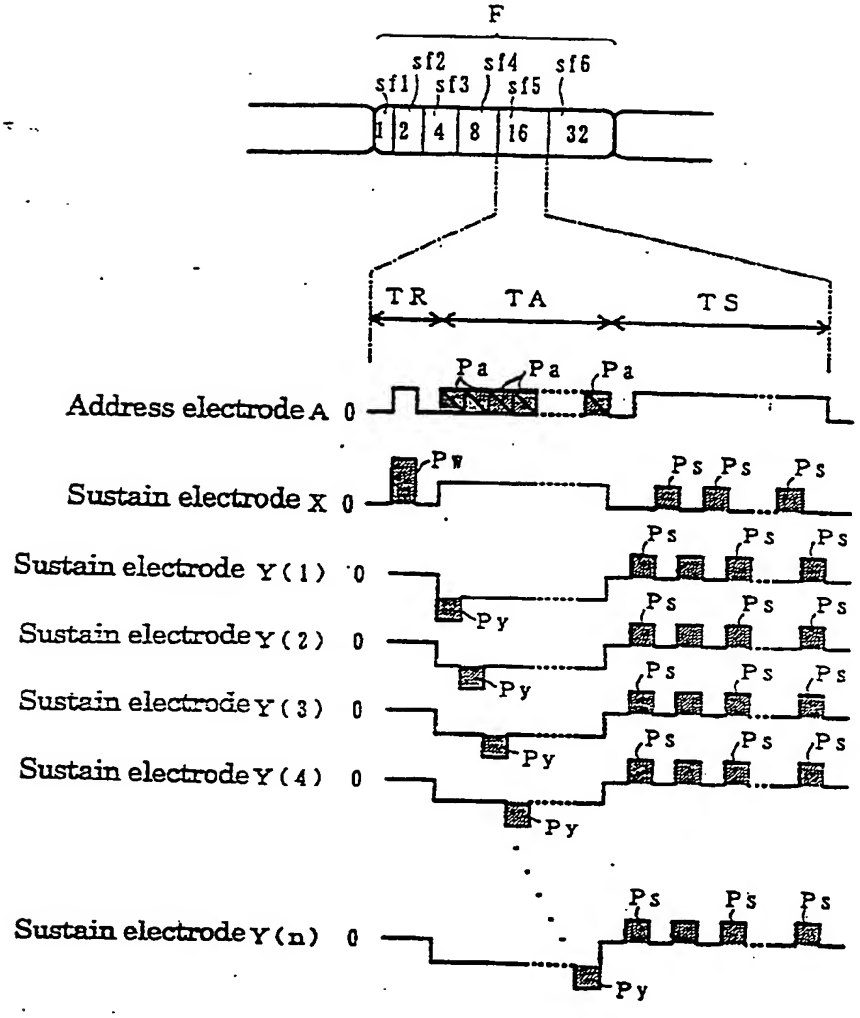

F
sf1
sf2
sf3
sf4
sf5
sf6
1
2
4
8
16
32
TR
TA
TS
Pa
Address electrode A
Pw
Ps
Sustain electrode X
Sustain electrode Y(1)
Sustain electrode Y(2)
Sustain electrode Y(3)
Sustain electrode Y(4)
Sustain electrode Y(n)
Py
0

Fig. 3

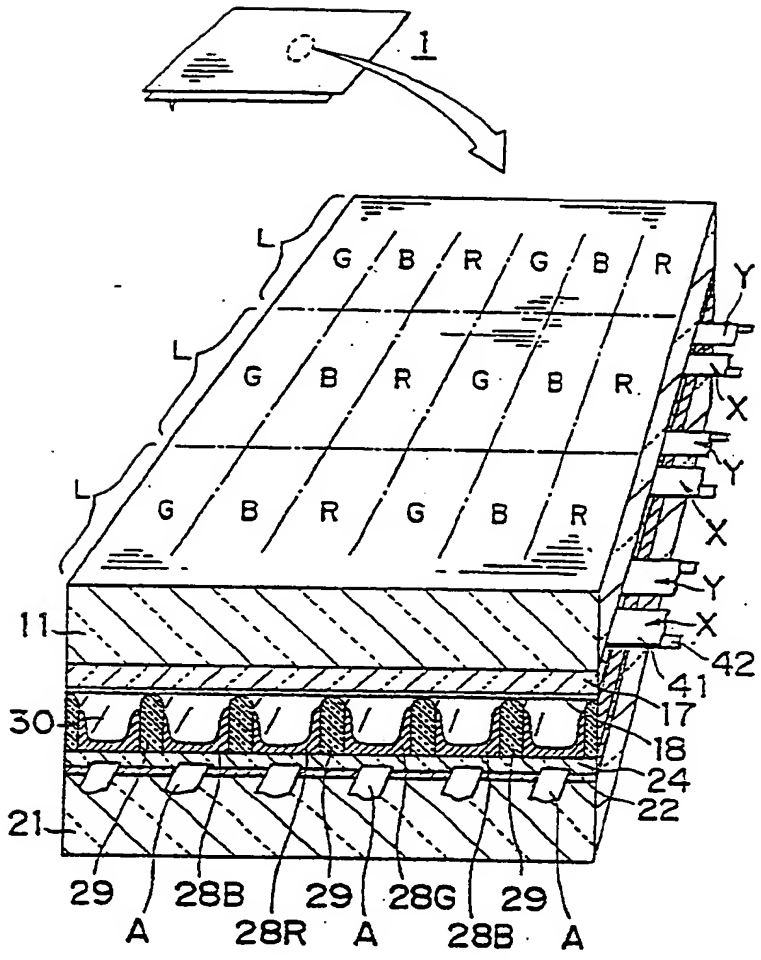


Fig. 4

Fig. 5(A)

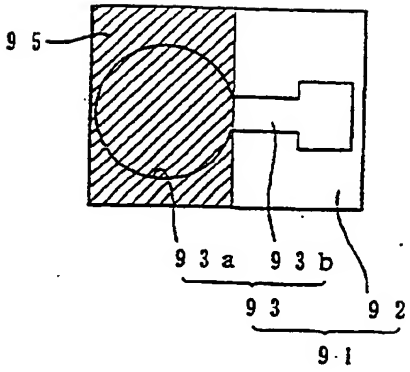
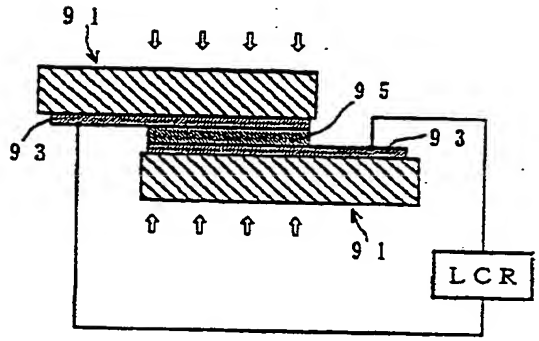


Fig. 5(B)



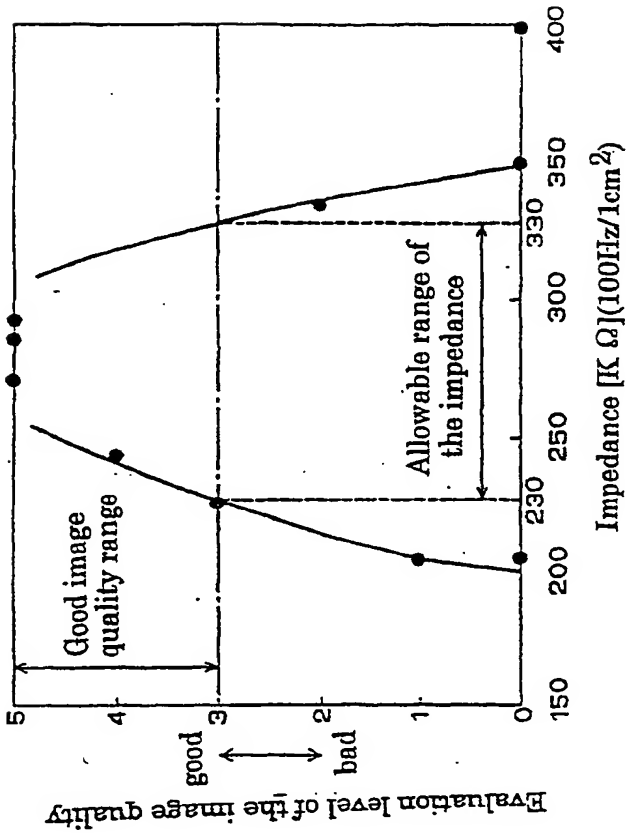

Evaluation level of the image quality
5
4
3
2
1
0
good
bad
Good image quality range
Allowable range of the impedance
150
200
230
250
300
330
350
400
Impedance [K Ω](100Hz/1cm²)

Fig. 6

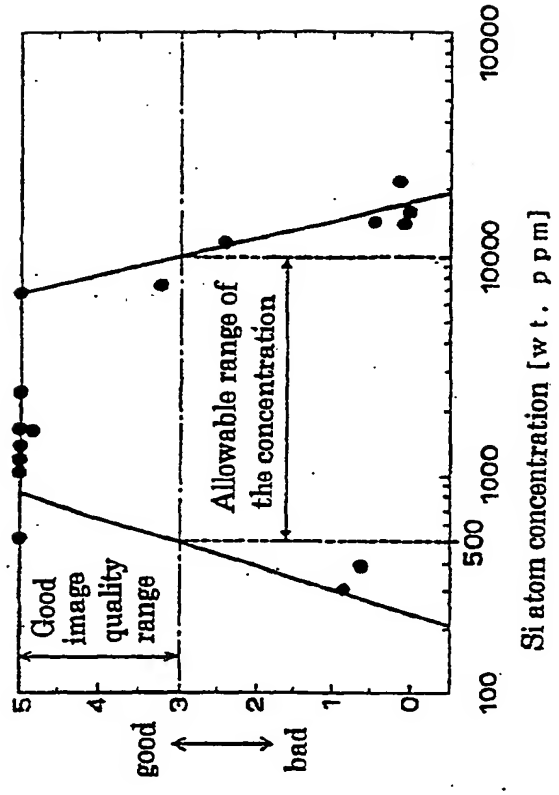

Good image quality range
Allowable range of the concentration
good
bad
5
4
3
2
1
0
100
500
1000
10000
10000
Si atom concentration [w t . p p m]

Fig. 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 02 6763

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 454 861 A (HASEGAWA HIROMI ET AL) 3 October 1995 (1995-10-03) * column 2, line 31 - line 52 * * column 3, line 9 - line 39; figure 1 * * column 7, line 26 - line 38 * * column 8, line 11 - line 21 *	1,3-6, 12,13	H01J17/04 H01J17/49 H01J9/02 C23C14/08
A	WO 96 37904 A (FUJITSU LTD ;AMATSU MASASHI (JP); KANAGU SHINJI (JP); SASAKA MASAA) 28 November 1996 (1996-11-28)	9-11	
P,A	& EP 0 788 131 A (FUJITSU LIMITED) 6 August 1997 (1997-08-06) * figure 1 * * column 7, line 35 - line 40 *	9-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01J
H01B
C03C
C23C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 February 2003	F de Ruyter-Noordman

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 02 6763

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

04-02-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5454861 A	03-10-1995	JP 3282882 B2	20-05-2002
		JP 6316671 A	15-11-1994
WO 9637904 A	28-11-1996	JP 9050769 A	18-02-1997
		DE 69624905 D1	02-01-2003
		EP 0788131 A1	06-08-1997
		WO 9637904 A1	28-11-1996
		KR 254479 B1	01-05-2000
		US 5977708 A	02-11-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82